RTCIO

TTL, A/D, D/A & Clock
I/O Expansion
for the RTC Series
Microcontrollers

Technical Manual

Release 1.1
5/15/89

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REAL-TIME CONTROLLER SERIES

The Real-Time Controller series system measures only 3.5 inches square and uses vertical-stacking connectors for I/O expansion. The RTC processor board contains the processor, EPROM and RAM memory, address decoding, buffering, parallel I/O with screw terminals, and an RS-232/RS-485 serial port. System expansion is through a pair of vertical-stacking headers, which eliminates the need for an expensive backplane.

The RTCIO board, the first in a series of I/O boards for the RTC series microcontrollers, contains three parallel TTL I/O ports and an 8-channel 8-bit A/D. Optional upgrades add a 4-channel 8-bit D/A, a battery-backed Real-Time Clock, and a DC-to-DC converter which allows complete 5-volt-only system operation.

A stacked-board arrangement has certain benefits besides eliminating costly gold-contact backplanes (motherboards). It allows configuration of either a basic system for experimentation or an expanded system for black-box applications yet still retains its low profile. Each vertically stacked board only increases the height by 5/8 inch. Additional cost can be saved by populating only the I/O necessary for the application.

VERTICAL-STACKING I/O EXPANSION

The vertical-stacking connectors pass all the necessary I/O control, address, and data signals to each expansion board added to the system. The buffered address/data bus (AD0-AD7), the latched address bus (A0-A7), and the upper four decoded address blocks (8000H, A000H, C000H & E000H) are grouped together. Control lines are bundled separately on a second vertical connector. These two connectors alone provide adequate mechanical stability for the stacking arrangement, but corner mounting holes are provided for #4 x 9/16" spacers.

JP16

	26	25	
Buffered D4			Buffered A3
Buffered D5			Buffered A2
Buffered D6			Buffered A1
Buffered D7			Buffered D0
+5 volts			+5 volts
Latched A4			Latched A3
Latched A5			Latched A2
Latched A6			Latched A1
Latched A7			Latched A0
+5 volts			+5 volts
0C000H			0A000H
0E000H			8000H
+12 volts			*GET
	2	1	

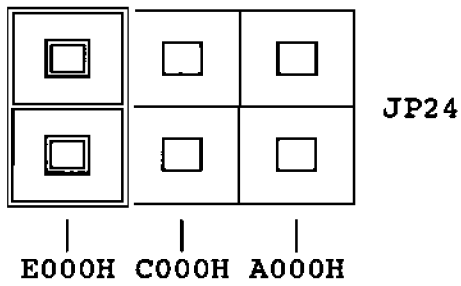
JP15

	26	25	
-12 volts			GND
ALE			GND
*DS			GND
*WR			GND
*RD			GND
*PSEN			GND
T1			*INT1
T0			*INT0
RESET			GND
P1.4			P1.3
P1.5			P1.2
P1.6			P1.1
P1.7			P1.0
	2	1	

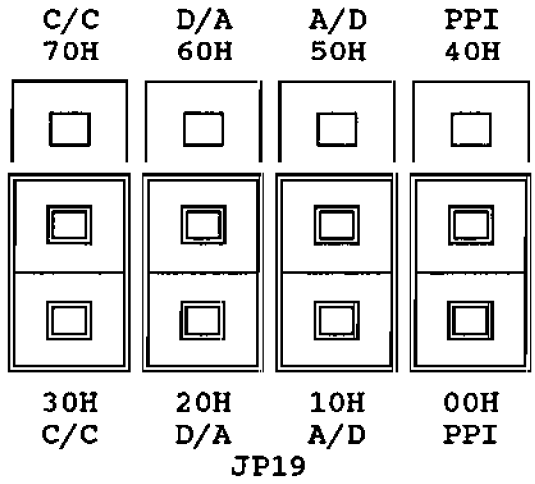
JP16 and JP15 bring the expansion bus up to I/O boards which mate atop the RTC series microcontrollers

SELECTING THE I/O ADDRESS SPACE

The RTC processor board decodes the address space into 8k blocks. The top three blocks (A000H-BFFFH, C000H-DFFFH, and E000H-FFFFH) are available for base address selection. U1, a 74HCT138 3-to-8 decoder, divides the selected base plus BAD7 intoo eight separate chip selects (xx0x-xx7x).



JP24 shows the LEFT jumper selecting the base address E000H



JP19 shows both jumpers down selecting:

JP24 E000H + 00H = E000H for the PPI
JP24 E000H + 10H = E010H for the A/D
JP24 E000H + 20H = E020H for the D/A
JP24 E000H + 30H = E030H for the C/C

The combination of these two jumpers (JP19 & JP24) makes it possible to address up to two of the RTCIO boards within the same 8K block of E000H. These default addresses (as shown above) will be adequate for most applications and the addresses used (in the examples) for the remainder of this manual.

TTL I/O

The 8255 programmable peripheral interface (PPI) is an efficient and cost-effective way to add TTL (logic level) I/O to any microcontroller system. The PPI adds 24 bits of I/O to the RTC system. The 24 bits are grouped into three 8-bit ports. Ports A & B can be independently programmed as 8-bit input or output ports. The third port, port C, is divided into two 4-bit nibbles (an upper and lower nibble). These nibbles can be programmed independently as 4-bit input or output ports.

The three ports are memory mapped. Referring to JP19 and JP24 we find the base + offset address of the PPI to be E000H + 00H (E000H). Starting with this address, the ports are addressed as follows:

8255 Port JP19 & JP24 address + 8255 offset address = actual address

Port A	E000H + 00H = E000H
Port B	E000H + 01H = E001H
Port C	E000H + 02H = E002H
Mode Port	E000H + 03H = E003H

The mode port is a write-only port used to set the PPI for the appropriate configuration. Let's assume we need 12 input bits and 12 output bits. Port A and the upper nibble of port C as inputs and port B and the lower nibble of port C as outputs. Writing a value of 98H to the mode port (E003H) configures the ports. Verify this value in the following chart:

PPI configuration values

Port A	Port C (upper) (nibble)	Port B	Port C (lower) (nibble)	Value
output	output	output	output	80H
output	output	output	input	81H
output	output	input	output	82H
output	output	input	input	83H
output	input	output	output	88H
output	input	output	input	89H
output	input	input	output	8AH
output	input	input	input	8BH
input	output	output	output	80H
input	output	output	input	91H
input	output	input	output	92H
input	output	input	input	93H
input	**input**	**output**	**output**	**98H**
input	input	output	input	99H
input	input	input	output	9AH
input	input	input	input	9BH

Once the PPI is configured the appropriate ports (A, B & C) can be read from and written to. In this example, reading port A (E000H) will return a value equal to the logic levels applied to the port A pins on JP17. Reading port C (E002H) will return a value equal to the logic levels applied to the upper nibble port C pins on JP17. The value returned for the upper nibble of port C will contain erroneous data in the lower nibble and must be discarded. ANDing the value read with 'F0H' will clear the lower nibble to zero.

Writing 'FFH' to port B (E001H) will set the corresponding bit pins on JP17 to a logic '1'. Writing '00H' to port C (E002H) will clear the corresponding bit pins on JP17 to a logic '0'. In this case the upper nibble is not used and could be any value.

Upon power-up or manual reset, the PPI is configured with all three ports (A, B, & C) as inputs. Once reconfigured, if necessary, for your application, care must be taken not to change the mode. The values at each port will be lost when the mode is changed.

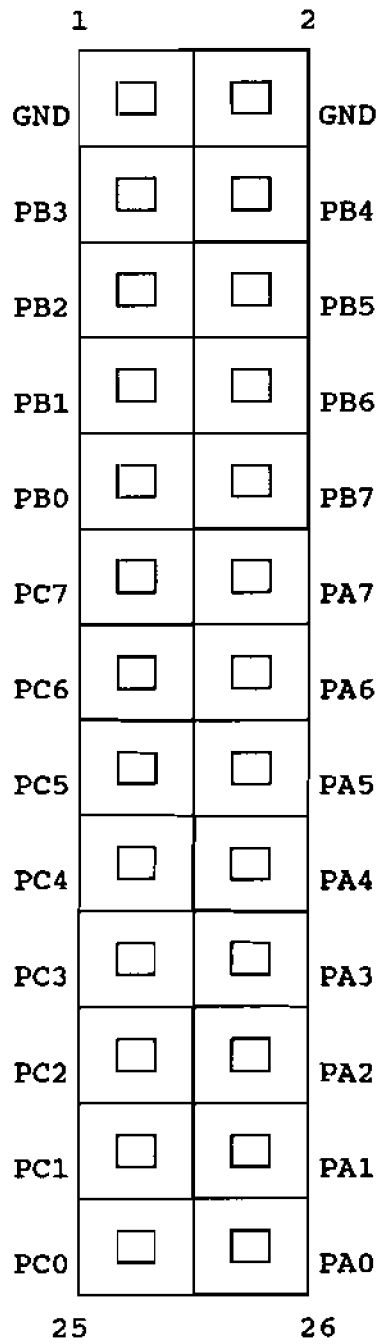
The 8255's port pins are brought out to connector JP17. JP17 is normally populated with a 2 x 13 right-angle square-pin header. These port pins can be brought directly up to the RTC-PROTO (prototyping) board by replacing the right-angle connector with a 2 x 13 straight pin header. This will simplify the wiring when DIP relays or opto-isolators are needed on the TTL I/O lines.

The following program, written for the RTC52, will allow easy configuration of the I/O ports and testing of your TTL I/O pins on JP17.

```
10      STRING 33,7
20     $(0)="OUTPUT" : $(1)="INPUT" : $(2)="WRITE" : $(3)="READ"
30     A=1 : B=1 : C=1
40     M=9BH : P=0E000H
50     PRINT
60     PRINT "Hit MENU Selection #"
70     PRINT "1 - Set Port A from ",$(A)," to ",$(ABS(A-1))
80     PRINT "2 - ",$(A+2)," PORT A"
90     PRINT "3 - Set Port B from ",$(B)," to ",$(ABS(B-1))
100     PRINT "4 - ",$(B+2)," PORT B"
110     PRINT "5 - Set Port C from ",$(C)," to ",$(ABS(C-1))
120     PRINT "6 - ",$(C+2)," PORT C"
130     PRINT "7 - END"
140   G=GET
150   G=GET
160    IF G=0 THEN 150
170   G=G-30H
180    IF ((G<1).OR.(G>7)) THEN 150
190    IF G=7 THEN  END
200    ON G-1 GOTO 1000,4000,2000,5000,3000,6000
```

```
999 REM ************************* Adjust Mode Port Value for Port A
1000    IF A=1 THEN 1050
1010   A=1
1020   M=M.OR.10H
1030    GOSUB 7000
1040    GOTO 50
1050   A=0
1060   M=M.AND.8FH
1070    GOSUB 7000
1080    GOTO 50
1999 REM ************************* Adjust Mode Port Value for Port B
2000    IF B=1 THEN 2050
2010   B=1
2020   M=M.OR.02H
2030    GOSUB 7000
2040    GOTO 50
2050   B=0
2060   M=M.AND.0FDH
2070    GOSUB 7000
2080    GOTO 50
2999 REM ************************* Adjust Mode Port Value for Port C
3000    IF C=1 THEN 3050
3010   C=1
3020   M=M.OR.09H
3030    GOSUB 7000
3040    GOTO 50
3050   C=0
3060   M=M.AND.0F6H
3070    GOSUB 7000
3080    GOTO 50
3999 REM ************************* Read/Write Port A
4000    IF A=1 THEN 4040
4010    INPUT "Enter Value"V
4020   XBY(P)=V
4030    GOTO 50
4040    PH0. XBY(P)
4050    GOTO 50
4999 REM ************************* Read/Write Port B
5000    IF B=1 THEN 5040
5010    INPUT "Enter Value"V
5020   XBY(P+1)=V
5030    GOTO 50
5040    PH0. XBY(P+1)
5050    GOTO 50
5999 REM ************************* Read/Write Port C
6000    IF C=1 THEN 6040
6010    INPUT "Enter Value"V
6020   XBY(P+2)=V
6030    GOTO 50
6040    PH0. XBY(P+2)
6050    GOTO 50
6999 REM ************************* Write Mode Port Value
7000  XBY(P+3)=M
7010   RETURN
```

Connector JP17 - PPI Port Pin Designation

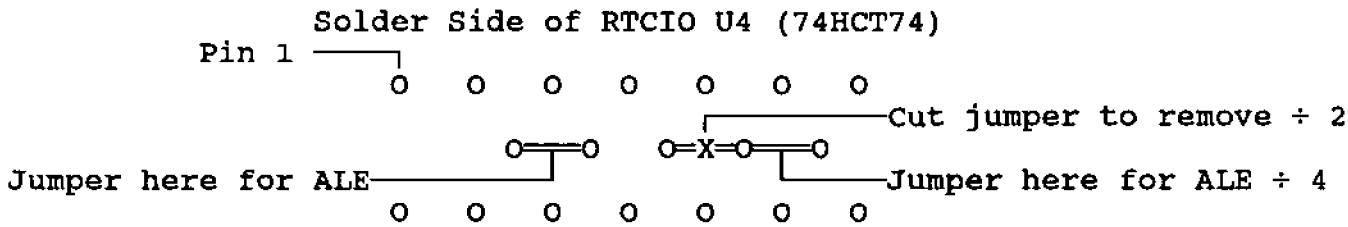


A/D INPUT

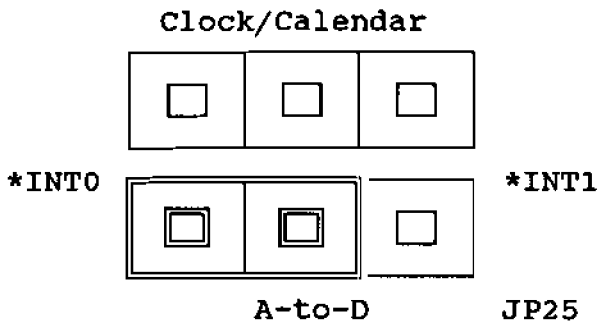
Control of a function often requires knowing more than whether it is off (logic 0) or it is on (logic 1). The ADC0808 A-to-D converter will provide this knowledge for eight separate input channels. The A/D requires only 5 volts for operation, although the 5.0-volt reference for the converter is regulated from +12V. The +12 volts must be provided by the user or by the optional on-board DC-to-DC converter. Trim-pot1 adjusts the 5.0-volt reference. The voltage range for all eight inputs is 0V-Vref (5.0V). Vref divided by the resolution of the A/D (8 bits, 255 steps) equals 19.6 millivolts/step.

NOTE: the A/D section requires +5V and +12V or +5V and the DC/DC option

The ALE line on the expansion bus is used to drive the clock input of the ADC0808. For example, on the RTC31/52 with an 11.0592-MHz crystal, the ALE line clocks at 1.8432 MHz. This exceeds the maximum input clock frequency of 1.28 MHz for the ADC0808. The RTCIO board provides a 74HCT74 (U4) used as a divide-by-two and -four. The divide-by-two output (921.6 kHz) is hard wired as clock input for the ADC0808. ALE and ALE divided by four are available for other RTC series microcontrollers to adjust maximum clock speed. This adjustment is accomplished by breaking the present connection and soldering a piece of wire appropriately as shown below:



The stock RTCIO using the default ALE divided by two, clocks the ADC0808 at 921.6 kHz. A conversion time of about 80 microseconds. End-of-conversion (EOC) is recognized in one of three ways. First, if using interpreted BASIC, the time it takes the system to start conversion and read back the results exceeds the EOC time, therefore EOC can be disregarded. Second, if using a compiled BASIC or machine language, a software loop of sufficient length can be inserted between the start of conversion and the read back to ensure the conversion is completed. Third, *INT0 or *INT1 can be used (JP25) to signal the RTC microcontroller of EOC. This produces the fastest response time. The EOC signal is inverted by Q2 and supplies a BUSY falling edge indicating an EOC.



JP25 shows *INT0 using the EOC signal (BUSY) as an interrupt source

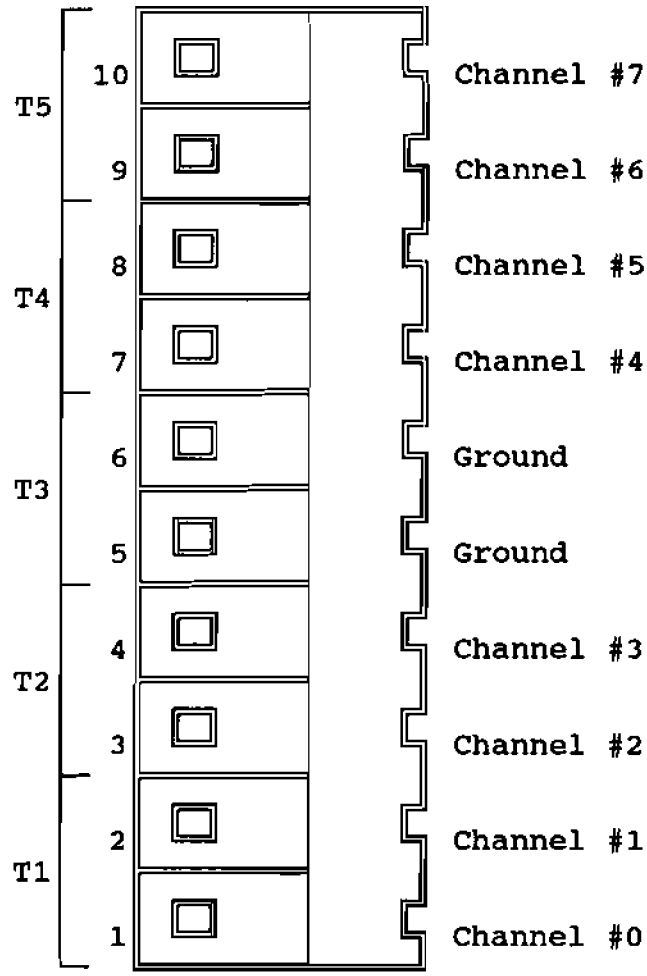
The base + offset address for the A/D as choosen earlier is E000H + 10H (E010H). The ADC0808 has eight input channels. The lower three latched address lines A0-A2 act as channel selects giving channels 0-7 the memory-mapped addresses of E010H + channel number (E010H-E017H).

The conversion is started by doing a dummy write to the address of the channel to convert. Writing 'xx' to address E013H starts a conversion for channel #3.

After EOC the converted value is read from any address within the E010H-E01FH range. Reading the value at address E010H will return the conversion value of the channel selected with the start of conversion command. To reduce confusion, it's a good idea to write to and read from the same address even though the read address can be any of the A/D's legal addresses.

Connections to the channel #0-7 inputs are made to the RTCIO board at T1-T5. Optional screw-terminal blocks make connections easily removable. Two connections, between channels #3 and #4, are at ground potential (-Vref).

NOTE: Exceeding 5V at any A/D input may permanently damage the ADC0808



Connections for A/D inputs channels #0-7 & Ground

The following program written for the RTC52 shows how easily the A/D is used. Attach inputs 0-5 volts (0-Vref) to an appropriate channel (#0-#7). Any unused channel which is not tied to ground will float and read as a good input. To avoid confusion, ground unused inputs.

```
190    PRINT "Channel     0   1   2   3   4   5   6   7"
200    PRINT "           ",
210    FOR X=0 TO 7
220   XBY(0E010H+X)=0
230    PH0. XBY(0E010H),
240    NEXT X
```

Changing line 230 to:

```
230   PRINT using(#.##),XBY(0E010H)*.0196,
```

...will display volts (0-5.00) instead of bit value (0-255)

ADJUSTMENT OF VREF

Pot1 will adjust Vref. Place the positive lead of a voltmeter on U3 pin 12 (+ref) and the negative lead on U3 pin 16 (-ref) and adjust Pot1 for 5.000 volts. Letting the circuit come to its operating temperature before making the adjustment will ensure minimum temperature drift.

OPTIONAL D/A OUTPUT

The natural progression from logic-level I/O to analog input conversion leads to analog output control. The AD7226 (U2) offers four channels of A-to-D conversion in a single package. Each output is buffered and capable of changing output levels at a rate of 3V/microsecond. The selection of each channel is accomplished with latched address bus A0-A1. Refering to JP19 and JP24 we find the base + offset address of the D/A to be E000H + 20H (E020H). Starting with this address, the output channels are addressed as follows:

D/A JP19 & JP24 address + D/A channel address = actual address

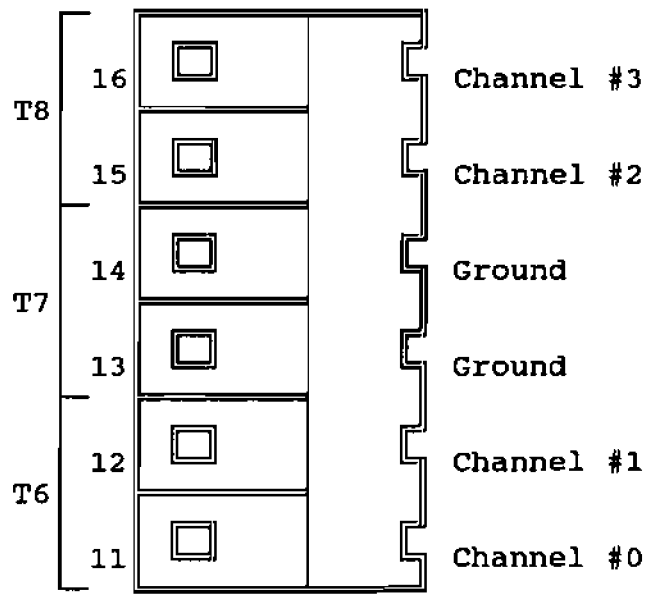
Channel #0	E020H + 00H = E020H
Channel #1	E020H + 01H = E021H
Channel #2	E020H + 02H = E022H
Channel #3	E020H + 03H = E023H

The AD7226 (D/A) uses the same Vref as the A/D: 5.00 volts. A negative voltage (Vss) is necessary to ensure the output can approach 0 volts, for data in of "zero". The -bias for Vss is obtained by zener Z2 from a -12 volt power supply. An optional on-board DC-to-DC converter will supply ±12 volts from the 5V supply.

NOTE: the D/A section requires +5V, +12V, and -12V or +5V and the DC/DC option

The resolution of the D/A is the same as the ADC0808 A/D: 8 bits. As calculated previously, this is 19.6 millivolts/bit. A data value of 102 (66H) will produce 2.00 volts (102 x .0196mA/bit) at the output. To do this, write the value to the appropriate channel address.

Connections to the channels #0-3 outputs are made to the RTCIO board at T6-T8. Optional screw-terminal blocks make connections easily removable. Two connections, between channel #1 and #2, are at ground potential (-Vref).



T5-T8 connections for the D-to-A channels #0-3 and Ground

This example program, written for the RTC52, incorporates both the A/D and the D/A. Tying channels #0-3 of the D-to-A to channels #0-3 of the A-to-D will close the loop and will read back whatever is written, ±1 bit.

```
10      PRINT
20      PRINT "Hit MENU Selection #"
30      PRINT "1 - Set D/A Channel 1"
40      PRINT "2 - Set D/A Channel 2"
50      PRINT "3 - Set D/A Channel 3"
60      PRINT "4 - Set D/A Channel 4"
70      PRINT "5 - Read A/D Channels 0-7"
80      PRINT "6 - End"
90     G=GET
100    G=GET
110     IF G=0 THEN 100
120    G=G-30H
130     IF ((G<1).OR.(G>6)) THEN 100
140     IF G=6 THEN  END
150     IF G=5 THEN 190
160     INPUT "Enter Value"V
170    XBY(0E020H+G-1)=V
180     GOTO 10
190     PRINT "Channel     0   1   2   3   4   5   6   7"
200     PRINT "           ",
210     FOR X=0 TO 7
220    XBY(0E010H+X)=0
230     PH0. XBY(0E010H),
240     NEXT X
250     PRINT
260     GOTO 10
```

NOTE: The output of each D/A channel can drive a 2K load. If the output voltage appears inaccurate when attached to external circuitry, make sure it is not overloading the output. Remove the external circuitry and verifying the output voltage again.

OPTIONAL REAL-TIME CLOCK/CALENDAR

Data collection and control applications are usually time dependent. The addition of a hardware clock/calendar can relieve the microcontroller from any timekeeping operations. OKI's M6242B CMOS clock/calendar (U7) has both a clock/calendar and selectable interrupt outputs. Thirteen registers hold time and date information and three registers are used for control purposes. These registers are addressed by the latched addresses A0-A3. Referring to JP19 and JP24 we find the base + offset address of the C/C to be E000H + 30H (E030H). Starting with this address, the output channels are addressed as follows:

C/C JP19 & JP24 address + C/C register address = actual address

```
Register  0 (S1)      E030H + 00H = E030H
Register  1 (S10)     E030H + 01H = E031H
Register  2 (MI1)     E030H + 02H = E032H
Register  3 (MI10)    E030H + 03H = E033H
Register  4 (H1)      E030H + 04H = E034H
Register  5 (H10)     E030H + 05H = E035H
Register  6 (D1)      E030H + 06H = E036H
Register  7 (D10)     E030H + 07H = E037H
Register  8 (MO1)     E030H + 08H = E038H
Register  9 (MO10)    E030H + 09H = E039H
Register 10 (Y1)      E030H + 0AH = E03AH
Register 11 (Y10)     E030H + 0BH = E03BH
Register 12 (W)       E030H + 0CH = E03CH
Register 13 (CD)      E030H + 0DH = E03DH  (control register D)
Register 14 (CE)      E030H + 0EH = E03EH  (control register E)
Register 15 (CF)      E030H + 0FH = E03FH  (control register F)
```

Each register is a nibble wide. The lower 4 bits of the data value are significant. Each value is between 0 and 15, most are from 0 to 9 (a decimal digit).

M6242B Clock/Calendar Register Table

Register #	Name	DATA D3	D2	D1	D0	DATA Limit	Description
0	S1	s8	s4	s2	s1	0-9	1-second digit
1	S10	**	s40	s20	s10	0-5	10-second digit
2	MI1	mi8	mi4	mi2	mi1	0-9	1-minute digit
3	MI10	**	mi40	mi20	mi10	0-5	10-minute digit
4	H1	h8	h4	h2	h1	0-9	1-hour digit
5	H10	**	PM/AM	h20	h10	0-2/0-1	PM/AM 10-hour digit
6	D1	d8	d4	d2	d1	0-9	1-day digit
7	D10	**	**	d20	d10	0-3	10-day digit
8	MO1	mo8	mo4	mo2	mo1	0-9	1-month digit
9	MO10	**	**	**	mo10	0-1	10-month digit
10	Y1	y8	y4	y2	y1	0-9	1-year digit
11	Y10	y80	y40	y20	y10	0-9	10-year digit
12	W	**	w4	w2	w1	0-6	week register
13	CD	30 sec	IRQ	BUSY	HOLD		control register D
14	CE	t1	t2	IRT/ST	MASK		control register E
15	CF	TEST	24/12	STOP	REST		control register F

There are two procedures for writing and reading clock/calendar information. Both procedures are similar with the exception of the hold and busy bits.

The first method involves setting the HOLD bit to a '1' and checking the BUSY bit. If the BUSY bit is '1' then reset the HOLD bit to '0' and start the sequence again. If the BUSY-bit is '0' then write or read any registers as needed. The HOLD bit should not exceed 1 second or it will be lost.

The second method disregards the HOLD and BUSY bits. The appropriate register is read from or written to and to ensure a proper read or write, a verify read must be performed. If a discrepancy is found, a correction is made and reverified.

Register Functions of the M6242B

S1, S10, MI1, MI10, H1, H10, D1, D10, MO1, MO10, Y1, Y10 & W

These registers are abbreviations for SECOND1, SECOND10, MINUTE1, MINUTE10, HOUR1, HOUR10, DAY1, DAY10, MONTH1, MONTH10, YEAR1, YEAR10, and WEEK. The values are in BCD notation (e.g. s8, s4, s2, s1 = 1001H or nine). Data values written outside the limit will cause erroneous readback results. The PM/AM bit must be set if using the 12-hour mode. Leap years are recognized and an illegal date will be corrected to the next correct date on the next day rollover. The days of the week are defined as:

w4	w2	w1	Weekday
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

Control D Register

HOLD **(D0)** Setting this bit to a '1' inhibits the 1-Hz S1 counter. A carry is held from the S1 counter until HOLD=0 providing HOLD isn't high greater than 1 second.

BUSY **(D1)** Status of interface condition. '1' indicates BUSY.

IRQ FLAG (D2) Status of the STD.P (OUT) output. '1' indicates an interrupt has occurred. Resetting this to a '0' will clear the interrupt. The IRQ FLAG must be a '1' when writing to the HOLD or 30 SEC bits of this control D register.

30 SEC (D3) Setting this bit to '1' will change the time to the closest whole minute. This bit will return to '0' when the clock/calendar can be accessed again. No reading from or writing to the time and day registers may be done during the 125 microseconds necessary to make this adjustment.

Control E Register

MASK (D0) This bit masks the STD.P output. Writing a '1' disables the output, '0' enables it.

IRT/ST (D1) This bit changes the STD.P mode. When this bit is a '1', normal interrupt mode is choosen. When this bit is a '0', a cyclic waveform is output determined by T0 and T1 (below).

T0 & T1 (D2 & D3) These bits select the cyclic waveform period of the interrupt line.

T0	T1	Period	Duty cycle of '0' level ('1' level = 7.8125 milliseconds)
0	0	1/64 second	1/2
0	1	1 second	1/128
1	0	1 minute	1/7680
1	1	1 hour	1/460800

Control F Register

REST (D0) A '1' written to this bit will clear the clock's internal divider counter of less than 1 second. A '0' will release the counter.

STOP (D1) A '1' written to this bit will stop all carries into the counter inhibiting timing. Writing a '0' enables carries (delay of 122 microseconds maximum depending on time for next carry).

24/12 (D2) A '1' indicates 24-hour mode (PM/AM invalid) and a '0' indicates 12-hour mode (PM/AM valid).
NOTE: The REST bit must be high to set the 24/12 mode.

TEST (D3) Setting this bit to a '1' clocks the seconds at 5416.3 Hz. This is for testing purposes only.

The following program, written for the RTC52, demonstrates the reading and writing of the M6242B.

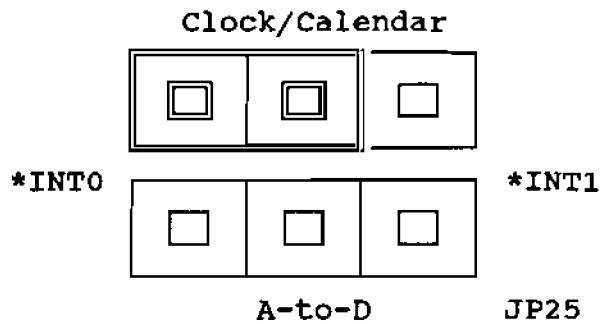
```
10     STRING 71,9 :  DIM T(15)
20  $(0)="Sunday" : $(1)="Monday" : $(2)="Tuesday" : $(3)="Wednesday"
30  $(4)="Thursday" : $(5)="Friday" : $(6)="Saturday"
40    XBY(0E03FH)=4
50     GOSUB 300
60     GOSUB 350
70     PRINT
80     PRINT "Hit MENU Selection #"
90     PRINT "1 - Set Seconds 0-59"
100    PRINT "2 - Set Minutes 0-59"
110    PRINT "3 - Set Hours 1-24"
120    PRINT "4 - Set Day 1-31"
130    PRINT "5 - Set Month 1-12"
140    PRINT "6 - Set Year 00-99"
150    PRINT "7 - Set Day of Week 0=Su 1=Mo 2=Tu 3=We 4=Th 5=Fr 6=Sa"
160    PRINT "8 - Read Clock & Calendar"
170    PRINT "9 - End"
```

```
180   G=GET
190   G=GET
200    IF G=0 THEN 190
210   G=G-30H
220    IF ((G<1).OR.(G>9)) THEN 190
230    IF G=9 THEN  END
240    IF G=8 THEN 50
250    INPUT "Enter Value"V
260    IF G=7 THEN 280
270   XBY(0E030H+(G*2)-1)=INT(V/10)
280   XBY(0E030H+(G*2)-2)=V-(INT(V/10)*10)
290    GOTO 50
297  REM ******************************************
298  REM * READ ALL THE TIME AND DATE REGISTERS
299  REM ******************************************
300    FOR X=0 TO 15
310   T(X)=(XBY(0E030H+X).AND.15)
320    IF (T(X)<>(XBY(0E030H+X).AND.15)) THEN 310
330    NEXT X
340    RETURN
347  REM ******************************************
348  REM * PRINT OUT CURRENT DATE AND TIME
349  REM ******************************************
350    PRINT $(T(12)),
360    PRINT 10*T(9)+T(8),"/",
370    PRINT 10*T(7)+T(6),"/",
380    PRINT 10*T(11)+T(10)," ",
390    PRINT 10*(T(5).AND.3)+T(4),":",
400    PRINT 10*T(3)+T(2),":",
410    PRINT 10*T(1)+T(0)
420    RETURN
```

This program does not check for legal entries. Enter values as prompted by the menu. The clock is set to the 24-hour mode.

NOTE: Powering the system up or down may cause an untimely write to the M6242B. A power-good signal produced by the DC-to-DC converter prevents this.

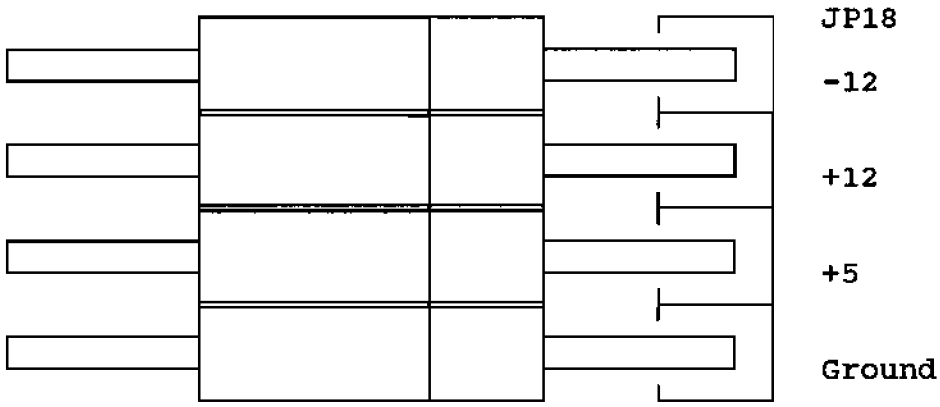
The STD.P output from the M6242B can be used as an interrupt source. The upper part of JP25 allows selection of either *INT0 or *INT1 for the interrupt. Two modes of interrupt can be selected through the control registers D-F of the M6242B. The IRT (interrupt) mode gives a one-time interrupt while the ST (standard) mode creates a recurring interrupt pulse. See the control register description for the particulars.



JP25 shows *INT0 using the STD.P signal as an interrupt source

OPTIONAL DC-TO-DC CONVERTER FOR 5-VOLT-ONLY OPERATION

The RTCIO board requires +12 volts to create the 5.00-volt reference for the A-to-D and D-to-A. In addition, the D-to-A requires +12 volts (actually +11.4V - +16.5V) and a -bias (-12V zenered to -4.7V). These voltages, +12V and -12V, can be user-supplied through JP18's right-angle Molex connector.



JP18 is a Molex-style 4-pin right-angle header

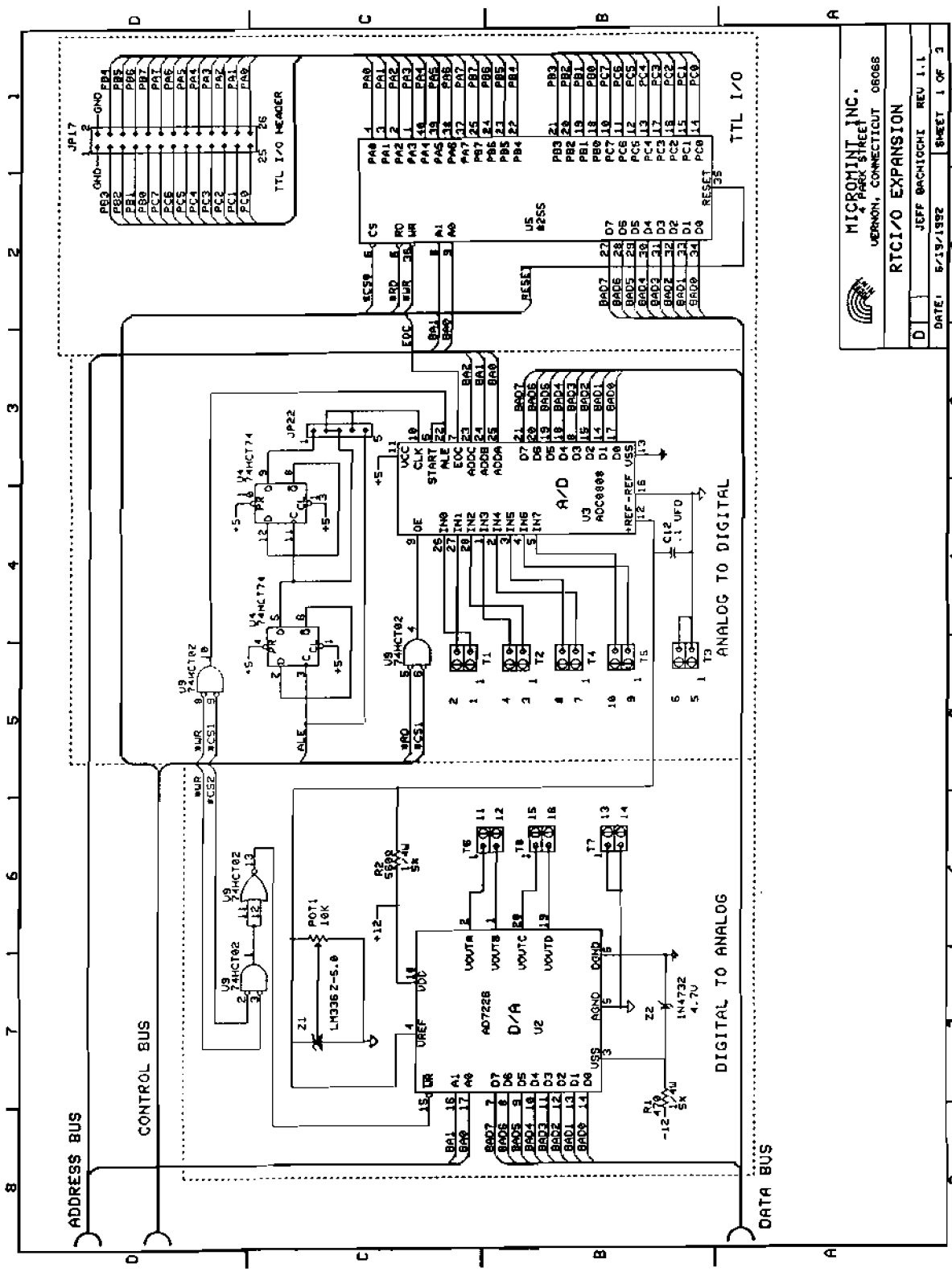
To eliminate the need for user supplied +12-volt and -12-volt power, the RTCIO board has an optional DC-to-DC converter. A +5-volt input is boosted to +15 volts by a MAX633 (U6) high-efficiency switching regulator.

The buffered internal oscilator (used for the swiching regulator) swings between ground and Vout (+15V). This output is used as a charge pump with capacitors C13 and C15 and diodes D3 and D4 to create -12 volts. The -12 volts supplies the -bias and the +15V (within the Vdd range) for the D-to-A. The +15 volts is also the source for the 5.00V Vref used by both the A-to-D and the D-to-A.

The DC-to-DC converter also contains additional circuitry. A low-Vcc detect circuit provides a *LBO (active-low Low Battery Output). Voltage divider R3 and R4 creates a +1.4-volt level from +5 volts. This voltage is compared to an internal reference of +1.31 volts and holds the *LBO line high. If the +5 volts drops to about +4.5 volts, the divider voltage will be reduced to +1.3 volts and the comparator will drive the *LBO line low. When the clock/calendar chip is battery backed, it stays active while the system's power is removed. The power fail detection is used to disable the M6242B clock/calendar chip prior to the system dropping power. If not disabled, the various data and control lines dropping may perform an unwanted write to the M6242B. This protection is somewhat reduced without the MAX633. Pull-up R5 holds the active-high CS1 enabled until +5 volts is dropped. It will then follow the supply down disabling the clock/calendar.

NOTE: using the components supplied, the DC-to-DC converter produces plus and minus voltage from 5 volts as follows:

Input	**Output**	**Output**
5 volts	+15 volts @ 20 mA	-12 volts @ 10 mA



RTCIO Schematics (1 of 3)